Claims

1-14 (Cancelled)

15. (Original) A receive block for asynchronous transfer mode (ATM) communications, comprising:

one or more cell delineation blocks each operable to receive an associated serial bit stream and each operable to identify ATM cell boundaries in the serial bit stream and convert one or more ATM cell payloads to parallel data;

a memory comprising one or more memory blocks, each of the memory blocks associated with one or more of the cell delineation blocks, wherein each memory block comprises one or more ATM cell storage locations;

a memory controller coupled to one or more of the cell delineation blocks and the memory, the memory controller operable to receive the parallel data from one or more of the cell delineation blocks and to communicate a portion of the parallel data to one or more of the cell storage locations in one or more of the memory blocks; and

a bus controller coupled to the memory controller and to the memory, the bus controller operable to interface with an ATM physical layer and to provide one or more signals to the memory for communicating one or more ATM cells via the ATM physical layer.

16. (Original) The receive block of Claim 15, wherein the bus controller is further operable to receive one or more address mode/select signals and to receive one or more subsets of port addresses via the ATM physical layer associated with the address mode/select signals.

17. (Original) The receive block of Claim 16, wherein one or more of the subsets each comprise four subsets of port addresses.

18. (Original) The receive block of Claim 15, wherein the cell delineation blocks comprise sixty-four cell delineation blocks.

19. (Original) The receive block of Claim 18, wherein the memory blocks comprise sixty-four memory blocks each with two ATM cell storage locations.

20. (Original) The receive block of Claim 15, wherein each cell delineation block comprises:

a cell delineation unit operable to receive the serial bit stream, the cell delineation unit identifying ATM cell boundaries and providing an output serial bit stream of an ATM cell payload;

a descrambler operable to receive the output serial bit stream of an ATM cell payload, the descrambler operable to descramble the bit stream; and

a serial/parallel converter operable to receive the descrambled bit stream, the serial/parallel converter operable to convert the bit stream to parallel data.

21. (Original) The receive block of Claim 15, wherein the ATM physical layer comprises a Utopia 2 interface.

22. (Original) The receive block of Claim 15, further comprising an ATM switch operable to receive communication from the bus controller and to further direct the communication to a destination via an ATM link.

23. (Original) A transmit block for asynchronous transfer mode (ATM) cell delineation, comprising:

a bus controller operable to interface with an ATM physical layer and to receive one or more ATM cells via the ATM physical layer;

one or more queue memories each comprising one or more cell storage locations;

one or more queue select devices each coupled to the bus controller and operable to receive output data from the bus controller, wherein the queue select devices are each operable to communicate the output data to each of the cell storage locations in an associated queue memory; and

one or more cell delineation blocks operable to receive parallel data from a selected associated queue memory, one or more of the cell delineation blocks being operable to convert the parallel data to a serial bit stream that comprises one or more ATM cells.

24. (Original) The transmit block of Claim 23, wherein the bus controller is further operable to receive one or more address mode/select signals and to receive one or more subsets of port addresses on the ATM physical layer associated with the address mode/select signals.

25. (Original) The transmit block of Claim 24, wherein one or more of the subsets comprise four subsets of port addresses.

26. (Original) The transmit block of Claim 23, wherein the cell delineation blocks comprise sixty-four cell delineation blocks.

27. (Original) The transmit block of Claim 23, wherein the queue memories comprise sixty-four queue memories each having two associated cell storage locations.

28. (Original) The transmit block of Claim 23, wherein each cell delineation block comprises:

a multiplexer operable to receive parallel data from the ATM cell storage locations in the associated queue memory, the multiplexer selecting one parallel data segment and providing it as an output;

a parallel/serial converter operable to receive the output from the multiplexer and to convert the parallel data segment to a serial bit stream; and

a descrambler operable to receive the serial bit stream and to scramble the serial bit stream and to provide the scrambled bit stream as an output.

29. (Original) The transmit block of Claim 23, wherein the ATM physical layer comprises a Utopia 2 interface.

30. (Original) The transmit block of Claim 23, further comprising an ATM switch operable to receive communication from the bus controller and to direct the communication to a destination via an ATM link.

31. (Original) An apparatus, comprising:

a bus controller operable to receive one or more asynchronous transfer mode (ATM) cells and from one or more memory blocks, wherein communication of the ATM cells from the bus controller is effected by a destination channel associated with an ATM signal that includes one or more of the ATM cells; and

a memory controller operable to communicate with the bus controller and to receive one or more ATM data streams, each of the data streams being associated with one or more of the memory blocks, wherein the memory controller is further operable to detect the status of one or more of the ATM cells and communicate that status to the bus controller such that at least some of the ATM cells that are stored in one or more of the memory blocks are communicated from a memory via one or more ATM links.

32. (Original) The apparatus of Claim 31, wherein one or more of the ATM cells are demultiplexed by one or more serial channels before they are communicated to the memory controller.

33. (Original) The apparatus of Claim 31, wherein the memory controller receives one or more of the ATM cells from a selected one of sixty-four serial channels, and wherein each of the serial channels has an associated cell delineation block.

34. (Original) The apparatus of Claim 31, wherein the bus controller and the memory controller each include software comprising verilog hardware description language.

35. (Original) The apparatus of Claim 31, wherein one or more of the ATM cells include a start of cell signal indicating a cell delineation protocol to be implemented.

36. (Original) The apparatus of Claim 31, wherein one or more of the ATM cells are operable to receive flow control information, the flow control information indicating a stop in transfer for one or more of the ATM cells received by the memory controller.

37. (Original) The apparatus of Claim 31, wherein one or more of the ATM cells each have a unique address that may be identified by the bus controller.

38. (Original) The apparatus of Claim 31, further comprising an ATM switch operable to receive communication from the bus controller and to direct the communication to a destination via an ATM link.

39. (Original) An apparatus, comprising:

a bus controller operable to receive one or more asynchronous transfer mode (ATM) data communication streams that include one or more ATM cells, the ATM communication streams being multiplexed and stored in one or more memory blocks, wherein the bus controller selects one or more of the ATM cells that are stored in one or more cell delineation blocks to be transferred to a destination based on data contained within one or more of the ATM cells, and wherein communication of one or more of the ATM cells is executed over a physical layer associated with the bus controller.

40. (Original) The apparatus of Claim 39, further comprising a memory controller operable to provide a status signal associated with one or more of the cell delineation blocks to the bus controller such that the bus controller generates a transmission signal to a memory, the transmission signal being received by the memory.

41. (Original) The apparatus of Claim 40, wherein one or more of the ATM cells are demultiplexed by one or more serial channels before they are communicated to the bus controller.

42. (Original) The apparatus of Claim 41, wherein the memory controller is coupled to the memory and the bus controller and is operable to receive one or more of the ATM cells from a selected one of sixty-four serial channels associated with the cell delineation blocks.

43. (Original) The apparatus of Claim 42, wherein the bus controller and the memory controller each include software comprising verilog hardware description language.

44. (Original) The apparatus of Claim 39, wherein one or more of the ATM cells include a start of cell signal indicating a cell delineation protocol to be implemented.

45. (Original) The apparatus of Claim 40, wherein one or more of the ATM cells are operable to receive flow control information, the flow control information indicating a stop in transfer for one or more of the ATM cells received by the memory controller.

46. (Original) The apparatus of Claim 39, wherein one or more of the ATM cells each have a unique address that may be identified by the bus controller.

47. (Original) The apparatus of Claim 39, further comprising an ATM switch operable to receive communication from the bus controller and to direct the communication to a destination via an ATM link.

48. (Original) A method comprising:

receiving a serial bit stream associated with one or more cell delineation blocks, wherein each of the cell delineation blocks is operable to identify ATM cell boundaries in the serial bit stream and convert one or more ATM cell payloads to parallel data;

receiving the parallel data from one or more of the cell delineation blocks with a memory controller and communicating a portion of the parallel data to one or more cell storage locations included in one or more memory blocks that are associated with one or more of the cell delineation blocks, wherein the memory blocks are included in a memory;

interfacing with an ATM physical layer using a bus controller; and

providing one or more signals to the memory for communicating one or more ATM cells via the ATM physical layer.

49. (Original) The method of Claim 48, further comprising demultiplexing one or more of the ATM cells with one or more serial channels before they are communicated to the memory controller.

50. (Original) The method of Claim 48, further comprising receiving, by the bus controller, one or more address mode/select signals and one or more subsets of port addresses via the ATM physical layer associated with the address mode/select signals.

51. (Original) The method of Claim 48, wherein the bus controller and the memory controller each include software comprising verilog hardware description language.

52. (Original) The method of Claim 48, wherein one or more of the ATM cells include a start of cell signal indicating a cell delineation protocol to be implemented.

53. (Original) The method of Claim 48, further comprising introducing flow control information to one or more of the ATM cells, the flow control information indicating a stop in transfer for one or more of the ATM cells received by the memory controller.

54. (Original) The method of Claim 48, wherein one or more of the ATM cells each have a unique address that may be identified by the bus controller.

55. (Original) The method of Claim 48, further comprising receiving, by an ATM switch, communication from the bus controller, wherein the ATM switch directs the communication to a destination via an ATM link.

56. (Original) The method of Claim 48, wherein the cell delineation blocks comprise sixty-four cell delineation blocks.

57. (Original) The method of Claim 48, further comprising:

receiving the serial bit stream with a cell delineation unit, the cell delineation unit identifying ATM cell boundaries and providing an output serial bit stream of an ATM cell payload;

receiving the output serial bit stream of an ATM cell payload with a descramble, the descrambler operable to descramble the bit stream; and

receiving the descrambled bit stream with a serial/parallel converter, the serial/parallel converter operable to convert the bit stream to parallel data.

58. (Original) The receive block of Claim 48, wherein the ATM physical layer comprises a Utopia 2 interface.

59. (Original) A method, comprising:

interfacing, with an ATM physical layer using a bus controller and receiving one or more ATM cells via the ATM physical layer;

receiving output data from the bus controller with one or more queue select devices, each coupled to the bus controller, wherein the queue select devices are each operable to communicate the output data to one or more cell storage locations in an associated queue memory, each of the cell storage locations included in one or more queue memories; and

receiving parallel data from a selected associated queue memory with one or more cell delineation blocks, one or more of the cell delineation blocks being operable to convert the parallel data to a serial bit stream that comprises one or more ATM cells.

60. (Original) The method of Claim 59, further comprising receiving, by the bus controller, one or more address mode/select signals and one or more subsets of port addresses on the ATM physical layer associated with the address mode/select signals.

61. (Original) The method of Claim 59, wherein the cell delineation blocks comprise sixty-four cell delineation blocks.

62. (Original) The method of Claim 59, wherein the queue memories comprise sixty-four queue memories each having two associated cell storage locations.

63. (Original) The method of Claim 59, wherein each cell delineation block comprises:

a multiplexer operable to receive parallel data from the ATM cell storage locations in the associated queue memory, the multiplexer selecting one parallel data segment and providing it as an output;

a parallel/serial converter operable to receive the output from the multiplexer and to convert the parallel data segment to a serial bit stream; and

a descrambler operable to receive the serial bit stream and to scramble the serial bit stream and to provide the scrambled bit stream as an output.

64. (Original) The method of Claim 59, wherein the ATM physical layer comprises a Utopia 2 interface.

65. (Original) The method of Claim 59, further comprising receiving, by an ATM switch, communication from the bus controller, wherein the ATM switch directs the communication to a destination via an ATM link.

66. (Original) Software embodied in a computer readable media and operable to:

receive a serial bit stream associated with one or more cell delineation blocks, wherein each of the cell delineation blocks is operable to identify ATM cell boundaries in the serial bit stream and convert one or more ATM cell payloads to parallel data;

receive the parallel data from one or more of the cell delineation blocks with a memory controller and communicating a portion of the parallel data to one or more cell storage locations included in one or more memory blocks that are associated with one or more of the cell delineation blocks, wherein the memory blocks are included in a memory;

interface with an ATM physical layer using a bus controller; and

provide one or more signals to the memory for communicating one or more ATM cells via the ATM physical layer.

67. (Original) The software of Claim 66, further operable to demultiplex one or more of the ATM cells with one or more serial channels before they are communicated to the memory controller.

68. (Original) The software of Claim 66, further operable to receive one or more address mode/select signals and one or more subsets of port addresses via the ATM physical layer associated with the address mode/select signals.

69. (Original) The software of Claim 66, wherein the bus controller and the memory controller each include software comprising verilog hardware description language.

70. (Original) The software of Claim 66, wherein one or more of the ATM cells include a start of cell signal indicating a cell delineation protocol to be implemented.

71. (Original) The software of Claim 66, further operable to introduce flow control information to one or more of the ATM cells, the flow control information indicating a stop in transfer for one or more of the ATM cells received by the memory controller.

72. (Original) The software of Claim 66, wherein one or more of the ATM cells each have a unique address that may be identified by the bus controller.

73. (Original) The software of Claim 66, further operable to receive, via an ATM switch, communication from the bus controller, wherein the ATM switch directs the communication to a destination via an ATM link.

74. (Original) The software of Claim 66, wherein the cell delineation blocks comprise sixty-four cell delineation blocks.

75. (Original) The software of Claim 66, further operable to:

receive the serial bit stream with a cell delineation unit, the cell delineation unit identifying ATM cell boundaries and provide an output serial bit stream of an ATM cell payload;

receive the output serial bit stream of an ATM cell payload with a descramble, the descrambler operable to descramble the bit stream; and

receive the descrambled bit stream with a serial/parallel converter, the serial/parallel converter operable to convert the bit stream to parallel data.

76. (Original) The software of Claim 66, wherein the ATM physical layer comprises a Utopia 2 interface.

77. (Original) Software embodied in a compute readable media and operable to:

interface, with an ATM physical layer using a bus controller and receive one or more ATM cells via the ATM physical layer;

receive output data from the bus controller with one or more queue select devices, each coupled to the bus controller, wherein the queue select devices are each operable to communicate the output data to one or more cell storage locations in an associated queue memory, each of the cell storage locations included in one or more queue memories; and

receive parallel data from a selected associated queue memory with one or more cell delineation blocks, one or more of the cell delineation blocks being operable to convert the parallel data to a serial bit stream that comprises one or more ATM cells.

78. (Original) The software of Claim 77, further operable to receive, via the bus controller, one or more address mode/select signals and one or more subsets of port addresses on the ATM physical layer associated with the address mode/select signals.

79. (Original) The software of Claim 77, wherein the cell delineation blocks comprise sixty-four cell delineation blocks.

80. (Original) The software of Claim 77, wherein the queue memories comprise sixty-four queue memories each having two associated cell storage locations.

81. (Original) The software of Claim 77, wherein the ATM physical layer comprises a Utopia 2 interface.

82. (Original) A system for asynchronous transfer mode (ATM) communications, comprising:

means for receiving a serial bit stream associated with one or more cell delineation blocks, wherein each of the cell delineation blocks is operable to identify ATM cell boundaries in the serial bit stream and convert one or more ATM cell payloads to parallel data;

means for receiving the parallel data from one or more of the cell delineation blocks with a memory controller and communicating a portion of the parallel data to one or more cell storage locations included in one or more memory blocks that are associated with one or more of the cell delineation blocks, wherein the memory blocks are included in a memory;

means for interfacing with an ATM physical layer using a bus controller; and

means for providing one or more signals to the memory for communicating one or more ATM cells via the ATM physical layer.

83. (Original) The system of Claim 82, further comprising means for demultiplexing one or more of the ATM cells with one or more serial channels before they are communicated to the memory controller.

84. (Original) The system of Claim 82, further comprising means for receiving, via the bus controller, one or more address mode/select signals and one or more subsets of port addresses via the ATM physical layer associated with the address mode/select signals.

85. (Original) The system of Claim 82, wherein the bus controller and the memory controller each include software comprising verilog hardware description language.

86. (Original) The system of Claim 82, wherein one or more of the ATM cells include a start of cell signal indicating a cell delineation protocol to be implemented.

87. (Original) The system of Claim 82, further comprising means for introducing flow control information to one or more of the ATM cells, the flow control information indicating a stop in transfer for one or more of the ATM cells received by the memory controller.

88. (Original) The system of Claim 82, wherein one or more of the ATM cells each have a unique address that may be identified by the bus controller.

89. (Original) The system of Claim 82, further comprising means for receiving, via an ATM switch, communication from the bus controller, wherein the ATM switch directs the communication to a destination via an ATM link.

90. (Original) The system of Claim 82, wherein the cell delineation blocks comprise sixty-four cell delineation blocks.

91. (Original) The system of Claim 82, further comprising:

means for receiving the serial bit stream with a cell delineation unit, the cell delineation unit identifying ATM cell boundaries and providing an output serial bit stream of an ATM cell payload;

means for receiving the output serial bit stream of an ATM cell payload with a descramble, the descrambler operable to descramble the bit stream; and

means for receiving the descrambled bit stream with a serial/parallel converter, the serial/parallel converter operable to convert the bit stream to parallel data.

92. (Original) The system of Claim 82, wherein the ATM physical layer comprises a Utopia 2 interface.

93. (Original) A system for asynchronous transfer mode (ATM) communications, comprising:

means for interfacing, with an ATM physical layer using a bus controller and receiving one or more ATM cells via the ATM physical layer;

means for receiving output data from the bus controller with one or more queue select devices, each coupled to the bus controller, wherein the queue select devices are each operable to communicate the output data to one or more cell storage locations in an associated queue memory, each of the cell storage locations included in one or more queue memories; and

means for receiving parallel data from a selected associated queue memory with one or more cell delineation blocks, one or more of the cell delineation blocks being operable to convert the parallel data to a serial bit stream that comprises one or more ATM cells.

94. (Original) The system of Claim 93, further comprising means for receiving, by the bus controller, one or more address mode/select signals and one or more subsets of port addresses on the ATM physical layer associated with the address mode/select signals.

95. (Original) The system of Claim 93, wherein the cell delineation blocks comprise sixty-four cell delineation blocks.

96. (Original) The system of Claim 93, wherein the queue memories comprise sixty-four queue memories each having two associated cell storage locations.

97. (Original) The system of Claim 93, wherein each cell delineation block comprises:

a multiplexer operable to receive parallel data from the ATM cell storage locations in the associated queue memory, the multiplexer selecting one parallel data segment and providing it as an output;

a parallel/serial converter operable to receive the output from the multiplexer and to convert the parallel data segment to a serial bit stream; and

a descrambler operable to receive the serial bit stream and to scramble the serial bit stream and to provide the scrambled bit stream as an output.

98. (Original) The system of Claim 93, wherein the ATM physical layer comprises a Utopia 2 interface.

99. (Original) The system of Claim 93, further comprising means for receiving, by an ATM switch, communication from the bus controller, wherein the ATM switch directs the communication to a destination via an ATM link.